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IEEE CNF IEEE Conference Proceeding

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☐ 1. **Design investigation of microprogrammable emulator architecture in distributed computer systems**

Deltchev, N.; Iliev, R.; Grantcharov, A.;
CompEuro '92 . 'Computer Systems and Software Engineering', Proceedings.
4-8 May 1992 Page(s):157 - 162

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IEEE CNF IEEE Conference Proceeding

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1. Impact of cycloconverter harmonics

Chu, R.F.; Burns, J.J.;

Industry Applications, IEEE Transactions on

Volume 25, Issue 3, May-June 1989 Page(s):427 - 435

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1. Impact of cycloconverter harmonics

Chu, R.F.; Burns, J.J.;

Industry Applications, IEEE Transactions on

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1 [Design of a user-microprogrammable building block](#)

Michael Krale, Randall Rettberg, Philip Herman, Robert Bressler, Anthony Lake

November 1980 **ACM SIGMICRO Newsletter , Proceedings of the 13th annual workshop on Microprogramming**, Volume 11 Issue 3-4

Full text available: pdf(956.02 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

A user-microprogrammable computer has been developed for use as a building block in general-purpose and dedicated computer systems. The architecture is designed to be easily microprogrammed and features a 32-bit, vertically oriented microinstruction. The processor has a 135-nanosecond cycle time, either 16- or 20-bit macro data paths, and 1024 hardware registers. A significant fraction of the processor bandwidth may be budgeted for I/O processing to allow the substitution of microcode for e ...

2 [Trace-driven memory simulation: a survey](#)

Richard A. Uhlig, Trevor N. Mudge

June 1997 **ACM Computing Surveys (CSUR)**, Volume 29 Issue 2

Full text available: pdf(636.11 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

As the gap between processor and memory speeds continues to widen, methods for evaluating memory system designs before they are implemented in hardware are becoming increasingly important. One such method, trace-driven memory simulation, has been the subject of intense interest among researchers and has, as a result, enjoyed rapid development and substantial improvements during the past decade. This article surveys and analyzes these developments by establishing criteria for evaluating trac ...

Keywords: TLBs, caches, memory management, memory simulation, trace-driven simulation

3 [The role of emulation in performance measurement and evaluation](#)

Liba Svobodova, Roy Mattson

March 1976 **Proceedings of the 1976 ACM SIGMETRICS conference on Computer performance modeling measurement and evaluation**

Full text available: pdf(840.52 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Emulation of systems makes it possible to combine the predictive power of simulation with the advantages of measurement carried under a real system workload. An emulator is a microprogrammed implementation of the basic hardware machine. It can be easily instrumented to collect performance statistics on the instruction set processor (ISP) level and support performance measurement of different configurations and software of the emulated system. This paper describes the monitoring capabilities ...


- 4 Trade-offs between communication throughput and parallel time
Yishay Mansour, Noam Nisan, Uzi Vishkin
May 1994 **Proceedings of the twenty-sixth annual ACM symposium on Theory of computing**

Full text available:  [pdf\(993.75 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

- 5 Disco: running commodity operating systems on scalable multiprocessors

Edouard Bugnion, Scott Devine, Kinshuk Govil, Mendel Rosenblum

November 1997 **ACM Transactions on Computer Systems (TOCS)**, Volume 15 Issue 4

Full text available:  [pdf\(400.76 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

In this article we examine the problem of extending modern operating systems to run efficiently on large-scale shared-memory multiprocessors without a large implementation effort. Our approach brings back an idea popular in the 1970s: virtual machine monitors. We use virtual machines to run multiple commodity operating systems on a scalable multiprocessor. This solution addresses many of the challenges facing the system software for these machines. We demonstrate our approach with a prototy ...

Keywords: scalable multiprocessors, virtual machines

- 6 Seismic modeling at 14 gigaflops on the connection machine

Jacek Myczkowski, Guy Steele


August 1991 **Proceedings of the 1991 ACM/IEEE conference on Supercomputing**

Full text available:  [pdf\(955.28 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

- 7 Preprototyping SIMD coprocessors using virtual machine emulation and trace compilation

Martin C. Herbordt, Owais Kidwai, Charles C. Weems

June 1997 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1997 ACM SIGMETRICS international conference on Measurement and modeling of computer systems**, Volume 25 Issue 1


Full text available:  [pdf\(2.05 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The use of massively parallel SIMD array architectures is proliferating in the area of domain specific coprocessors. Even so, they have undergone few systematic empirical studies. The underlying problems include the size of the architecture space, the lack of portability of the test programs, and the inherent complexity of simulating up to hundreds of thousands of processing elements. We address the computational cost problem with a novel approach to trace-based simulation. Code is run on an abs ...

- 8 Separating data and control transfer in distributed operating systems

Chandramohan A. Thekkath, Henry M. Levy, Edward D. Lazowska

November 1994 **Proceedings of the sixth international conference on Architectural support for programming languages and operating systems**, Volume 29, 28 Issue 11, 5


Full text available:  [pdf\(1.42 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Advances in processor architecture and technology have resulted in workstations in the 100+ MIPS range. As well, newer local-area networks such as ATM promise a ten- to hundred-fold increase in throughput, much reduced latency, greater scalability, and greatly increased reliability, when compared to current LANs such as Ethernet. We believe that these new network and processor technologies will permit tighter coupling of distributed systems at the hardware level, and that distribu ...

Sharing memory robustly in message-passing systems

Hagit Attiya, Amotz Bar-Noy, Danny Dolev

January 1995 **Journal of the ACM (JACM)**, Volume 42 Issue 1

Full text available:  [pdf\(1.44 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)


Emulators that translate algorithms from the shared-memory model to two different message-passing models are presented. Both are achieved by implementing a wait-free, atomic, single-writer multi-reader register in unreliable, asynchronous networks. The two message-passing models considered are a complete network with processor failures and an arbitrary network with dynamic link failures. These results make it possible to view the shared-memory model as a higher-level language for ...

Keywords: atomic registers, emulation, fault-tolerance, message passing, processor and link failures, shared memory, wait-freedom

10 The evolution of the Sperry Univac 1100 series: a history, analysis, and projection

B. R. Borgerson, M. L. Hanson, P. A. Hartley

January 1978 **Communications of the ACM**, Volume 21 Issue 1

Full text available:  [pdf\(1.89 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [citations](#), [index terms](#)

The 1100 series systems are Sperry Univac's large-scale mainframe computer systems. Beginning with the 1107 in 1962, the 1100 series has progressed through a succession of eight compatible computer models to the latest system, the 1100/80, introduced in 1977. The 1100 series hardware architecture is based on a 36-bit word, ones complement structure which obtains one operand from storage and one from a high-speed register, or two operands from high-speed registers. The 1100 Operating System ...

Keywords: 1100 computer series, computer architecture, data management systems, end user facilities, executive control software, multiprocessing, multiprogramming, operating system, programming languages

11 Design considerations for a QM-1 based multimicroprocessor emulation system

Steve Crocker

November 1978 **ACM SIGMICRO Newsletter , Proceedings of the 11th annual workshop on Microprogramming**, Volume 9 Issue 4

Full text available:  [pdf\(83.98 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [index terms](#)

Microprocessors, which are now readily available, are being used in the design of many systems. Soon avionic systems will be designed that use many microprocessors working together. Systems based on multiple microprocessors (MMP) will be designed to offer higher throughput and/or higher reliability than uniprocessor systems. There are now very few design tools to aid in developing or evaluating proposed microprocessor systems. One highly useful tool is an emulation facility for m ...

12 Emulation of computer networks by microprogrammable microcomputers

David Cohen, Ming T. Liu

September 1974 **Conference record of the 7th annual workshop on Microprogramming**

Full text available:  [pdf\(430.27 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The advent of low cost, sophisticated, microprogrammable, LSI microprocessors has renewed interest in multiple-computer systems. This paper suggests a method of implementing microprogrammable microcomputer systems as a sophisticated tool (emulators) for decreasing the economic risk involved in development of large computer networks. Two levels of emulation are proposed for different network configurations. At the first level each microprocessor emulates one of the large computers in the rea ...

13 A quantitative analysis of locality in dataflow programs

William Marcus Miller, Walid A. Najjar, A. P. Wim Böhm

September 1991 **Proceedings of the 24th annual international symposium on**


Microarchitecture

Full text available:  [pdf\(616.29 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

14 System description of the JHU emulation laboratory

Charles Neuhauser

September 1974 **Conference record of the 7th annual workshop on Microprogramming**


Full text available:  [pdf\(364.41 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The emulation laboratory described in this paper is being implemented at Johns Hopkins University as a research and educational facility. Currently, we are planning to use this laboratory to support research in the following areas: 1) Examination of and experimentation with novel system architectures, 2) Evaluation of various directly executed language (DEL) structures and the effective structure of their associated base machines [4], and 3) Dynamic analysis ...

15 A high level multi-lingual multiprocessor KMP/II

Mario Tokoro, Kiichiro Tamaru, Masaaki Mizuno, Masao Hori

May 1980 **Proceedings of the 7th annual symposium on Computer Architecture**

Full text available:  [pdf\(758.22 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

KMP/II is a multiprocessor system designed to work as a multi-lingual high level language computer in a distributed processing environment. The multiprocessor system is composed of up to 15 dynamically microprogrammable LSI processors. One processor executes OS functions. Another processor executes I/O functions. All the rest execute user programs as high level language job processors, emulating individual high level language. Allocation of high level language emulators to processors change ...

16 A virtual machine emulator for performance evaluation

M. D. Canon, D. H. Fritz, J. H. Howard, T. D. Howell, M. F. Mitoma, J. Rodriguez-Rosell

February 1980 **Communications of the ACM**, Volume 23 Issue 2



Full text available:  [pdf\(865.59 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#)

Keywords: computer system simulation, performance evaluation, virtual machines

17 Is SC + ILP = RC?

Chris Gniady, Babak Falsafi, T. N. Vijaykumar

May 1999 **ACM SIGARCH Computer Architecture News , Proceedings of the 26th annual international symposium on Computer architecture**, Volume 27 Issue 2


Full text available:  [pdf\(94.62 KB\)](#)  Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)
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Sequential consistency (SC) is the simplest programming interface for shared-memory systems but imposes program order among all memory operations, possibly precluding high performance implementations. Release consistency (RC), however, enables the highest performance implementations but puts the burden on the programmer to specify which memory operations need to be atomic and in program order. This paper shows, for the first time, that SC implementations can perform as well as RC implementations ...

18 Implementation of high speed data sets with microprogrammable data processors

Glenn N. Caplin, Anne R. Clayton, Richard L. Stuart

November 1978 **ACM SIGMICRO Newsletter , Proceedings of the 11th annual workshop on Microprogramming**, Volume 9 Issue 4

Full text available:  [pdf\(448.39 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Modern high speed data sets (or Modems) are usually required to perform a great deal of

digital signal processing to maintain acceptable error rates for worst-case channel conditions. Previously, this digital processing task was implemented with dedicated SSI/MSI TTL circuits. With the advent of high speed microprogrammable units (ALU's, sequencers, etc.), it has become possible to replace a random logic design with a functionally equivalent microprogrammed design. This results in better de ...

19 The rice parallel processing testbed

R. C. Covington, S. Madala, V. Mehta, J. R. Jump, J. B. Sinclair

May 1988 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1988 ACM SIGMETRICS conference on Measurement and modeling of computer systems**, Volume 16 Issue 1


Full text available:  [pdf\(577.24 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)



20 The development of user microprogramming: A survey and status report

Richard T. Thomas

September 1974 **Conference record of the 7th annual workshop on Microprogramming**

Full text available:  [pdf\(451.17 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)







Over the past few years there has been an increasing interest in user microprogramming. This paper traces the development of user microprogramming, surveying several different modifications made to commercially available microprogram control computers. A brief overview is given of various proposals for machines allowing user microprogramming as a basic design goal. Also, several contemporary machines which allow user microprogramming are discussed. The various microprogramming facilities pr ...

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1 [The NuMesh: a modular, scalable communications substrate](#)

Steve Ward, Karim Abdalla, Rajeev Dujari, Michael Fetterman, Frank Honoré, Ricardo Jenez, Philippe Laffont, Ken Mackenzie, Chris Metcalf, Milan Minsky, John Nguyen, John Pezaris, Gill Pratt, Russell Tessier

August 1993 **Proceedings of the 7th international conference on Supercomputing**


Full text available:  [pdf\(1.02 MB\)](#)

Additional Information: [full citation](#), [references](#), [index terms](#)

2 [The DOWL distributed object-oriented language](#)

Bruno Achauer

September 1993 **Communications of the ACM**, Volume 36 Issue 9

Full text available:  [pdf\(2.55 MB\)](#)


Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

Keywords: concurrency, concurrent object-oriented programming

3 [The muse object architecture: a new operating system structuring concept](#)

Yasuhiko Yokote, Fumio Teraoka, Atsushi Mitsuzawa, Nobuhisa Fujinami, Mario Tokoro

April 1991 **ACM SIGOPS Operating Systems Review**, Volume 25 Issue 2

Full text available:  [pdf\(1.92 MB\)](#)


Additional Information: [full citation](#), [abstract](#), [citations](#), [index terms](#)

A next generation operating system should accommodate an ultra large-scale, open, self-advancing, and distributed environment. This environment is dynamic and versatile in nature. In it, an unlimited number of objects, ranging from fine to coarse-grained, are emerging, vanishing, evolving, and being replaced; computers of various processing capacities are dynamically connected and disconnected to networks; systems can optimize object execution by automatically detecting the user's and/or program ...

4 [Automated synthesis of interface adapters for reusable classes](#)

Satish R. Thatté

February 1994 **Proceedings of the 21st ACM SIGPLAN-SIGACT symposium on Principles of programming languages**

Full text available:  [pdf\(1.37 MB\)](#)


Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The need to fit together reusable components and system designs in spite of differences in protocol and representation choices occurs often in object-oriented software construction. It is therefore necessary to use adapters to achieve an exact fit between the available "socket" for a reusable part and the actual part. In this paper we discuss an approach to the construction of tools that largely automate the synthesis of adapter code. Such tools ...

5 An interpretation of objects and object types

Martin Abadi, Luca Cardelli, Ramesh Viswanathan

January 1996 **Proceedings of the 23rd ACM SIGPLAN-SIGACT symposium on Principles of programming languages**

Full text available:  [pdf\(1.21 MB\)](#)


Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)



6 Coping with type casts in C

Michael Siff, Satish Chandra, Thomas Ball, Krishna Kunchithapadam, Thomas Reps

October 1999 **ACM SIGSOFT Software Engineering Notes , Proceedings of the 7th European software engineering conference held jointly with the 7th ACM SIGSOFT international symposium on Foundations of software engineering**, Volume 24 Issue 6

Full text available:  [pdf\(1.32 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The use of type casts is pervasive in C. Although casts provide great flexibility in writing programs, their use obscures the meaning of programs, and can present obstacles during maintenance. Casts involving pointers to structures (C structs) are particularly problematic, because by using them, a programmer can interpret any memory region to be of any desired type, thereby compromising C's already weak type system. This paper presents an approach for making sense of such casts, i ...



7 Teaching experimental design in an operating systems class

Allen B. Downey

March 1999 **ACM SIGCSE Bulletin , The proceedings of the thirtieth SIGCSE technical symposium on Computer science education**, Volume 31 Issue 1

Full text available:  [pdf\(588.84 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)





This paper describes an operating systems (OS) class that departs from more common approaches by introducing experimental design explicitly as part of the course material. Instead of implementing operating systems components or modifying existing operating systems, students conduct a series of experiments that measure the performance of system services and try to infer information about their implementation from the results. These experiments reinforce the OS concepts presented in lecture, and a ...



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1 [Technical contributions: Pascal and comms programming](#)

Jan E. Jonak

April 1985 **ACM SIGPLAN Notices**, Volume 20 Issue 4


Full text available:  [pdf\(694.71 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#)

Complex architectures of specialised processors are not always easily amenable to high level language programming without having to pay high price in terms of poor resources utilisation or lengthy custom language design and compiler development process. This paper describes Pascal-F, an attempt at a minimal modification of the widely accepted language Pascal to achieve close match between source and object code in a specialised communications processor and to make possible transportation of at le ...

2 [Experience with a FORTH-like language](#)

J E Jonak

February 1986 **ACM SIGPLAN Notices**, Volume 21 Issue 2


Full text available:  [pdf\(694.37 KB\)](#) Additional Information: [full citation](#), [abstract](#), [index terms](#)

Extensible and threaded code language FORTH is very popular among amateur programmers but only few professionals admit they use it or are prepared to describe their experience. The author has been using a directly threaded variation of FORTH, called F, for development of a couple of software products. And although convinced of the language usefulness as an implementation tool he would like to point out a few problem areas which he encountered during the development and life time of these products ...

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museum +art

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IBM images.

The two problems that have to be solved are the terminal emulation and the network ... product called the DCP/88 **Distributed Communications Processor**. ...

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Military Acronyms, Initialisms, and Abbreviations

DCP-40 **Distributed Communications Processor**, Model 40 ... DSEA 1display station emulation adapter, 2data storage electronics assembly ...

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007 James Bond 007 1TR6 (Ger) FTZ regulation (close to CCITT Q.930 ...

... [GEC] DCP **Distributed Communications Processor** DCP Duplex Central Processor DCPR ... DOSEM DOS Emulation DOST Disc Operating System for Testing [GEC] ? ...

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Computer Acronym List v3.00 This is a list of computer acronyms ...

... for Critical Parts DCP **Distributed Communications Processor** DCP Duplex ... Single-layer Embedded DSEA Display Station Emulation Adapter DSECT Dummy ...

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International Information Retrieval Guild <= The Hackers Acronym ...

... for Critical Parts DCP **Distributed Communications Processor** DCP Duplex ... Data Module DTE Data Terminal Emulation DTE Data Terminal Equipment DTF Dial ...

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FB-Informatik (TU-KL) -- English Acronyms

... Order DCP - **Distributed Communications Processor** DCP - Duplex Central ...

End Office Toll Trunking EP - **Emulation** Program EP - Experience Points EP ...

sci.informatik.uni-kl.de/mitarbeiter/thees/acronyms/body.html - 101k - Jun 4, 2005 - [Cached](#) - [Similar pages](#)

AAA Abdominal Aortic Aneurysm AAA Access All Areas AAA Access ...

... Event Mechanism AEM Automatic **Emulation** Management AEN Alberta Environmental

... DCP Display Control Panel DCP **Distributed Communications Processor** DCP ...

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CS Hypertext Glossar - D

DBCES - Dynamic Bandwidth by Circuit **Emulation** Services (ATM). DBCS - [1] Delivery

Bar Code Sorter ... DCP - [1] **Distributed Communications Processor** ...

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faster on the 1108 than IBM's 7094 emulation. did on the 360. Sperry Rand had a program that ... **Distributed Communications Processor** (DCP) ...

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NIC 50002 DDN PROTOCOL IMPLEMENTATIONS AND VENDORS GUIDE February ...

TELNET sessions provide VT100 terminal emulation and may be recorded in a ...

in the mainframe and partly in the **Distributed Communications Processor** (DCP). ...

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